REMARKS

Based on the above amendment and the following remarks, applicant respectfully submits that all the pending claims are in condition for allowance.

Status of the Claims

Claims 1-8, 10-15 were pending.

Claim 16-24 have been added.

Claims 1-8, 10-15, 16-24 are now pending

Rejections under 35 USC § 102

The standard for a rejection under 35 USC § 102 is anticipation. "To anticipate a claim, the reference must teach every element of the claim." MPEP 2131. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

The examiner rejected claim 15 under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,141,718 ("Garnett et al."). Applicants traverse the 102(e) rejection to claim 15 for the reasons specified below.

First, the examiner cites Garnett et al. as teaching "a plurality of local busses each for transferring data between a processing device and an associated memory module." Specifically, the examiner cites busses (fig. 2, 22, 24, 26) as transferring data between a processing device (fig. 2, 14, 16) and an associated memory module (DMA, 133). The memory module (DMA, 133) cited by the examiner is **not** associated with a particular processing device (fig. 2, 14, 16) as required by claim 15. Specifically, Garnett et al. teaches that the DMA memory is located inside the bridge (fig. 1, 12) and is used for controlling operation of the bridge (see col. 15, lines 7-24).

Accordingly, the DMA memory cited by the examiner is associated with the bridge (fig. 1, 12) and not the processing devices (14, 16 of fig. 2) as required by claim 15.

Second, as taught in Garnett, the referred to busses (22, 24, 26 of fig.2) are I/O busses (see col. 4, lines 62-67, col. 5, lines 1-10) and are not local busses between a processing device and an associated memory module as required in claim 15. Applicants submit a local bus is a relatively high performance bus for transferring data between a processor and its associated memory. In contrast, I/O busses are relatively low-speed busses that transfer data to and from peripheral devices. For at least these reasons individually or in combination, applicants submit that independent claim 15 is allowable over the cited art.

Rejections Under 35 USC § 103

The examiner rejected claims 1-8, 10-14 under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 6,141,718 ("Garnett et al.").

To reject a claim under 35 USC § 103, the examiner must establish prima facie obviousness. One factor required to establish prima facie obviousness of a claimed invention is that all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981 (CCPA 1974). See MPEP 2143.03. Applicant traverses the §103 rejections and respectfully submits that the examiner has not established a prima facie case of obviousness because the cited art does not teach or suggest all the claim limitations.

Claim 1 recites in part, "the bus bridges each include a set of multiplexers." The examiner admits Garnett et al. does not teach a set of mutiplexers and states "mere duplication of the essential working parts of a device involves only routine skill in the art" without citing any support for the assertion. Applicants respectfully traverse this rejection and call for the examiner to support this rejection with citation to an independent reference in accordance with MPEP 706.02 and 2144.03.

Claim 1 recites in part, "the bus bridges include a multiplexer for each outgoing bit line." Garnett et al. does not teach this limitation. Specifically, Garnett teaches a bridge (fig. 1, 12) that couples to multiple output bit lines (fig. 2, 22, 24, 26). However, the bridge (fig. 1, 12) only uses one multiplexer (fig. 9, 143).

The use of a mutliplexer for each outgoing bit line as required in claim 1 provides a configurable high-speed connection at each intersection of "a plurality of busses" and "at least one cross-bus" as cited in claim 1. Applicants submit that using only one multiplexer in a bridge as taught in Garnett would substantially change performance and control of each bridge. For at least these reasons individually or in combination, applicants submit claim 1 is allowable over the cited art.

Claims 2-8, and 10 depend from claim 1. Applicants respectfully submit that claim 1 and its dependent claims 2-8, and 10 are allowable over the cited art for the reasons given above.

Claim 11 recites in part, "the bus bridges each include a multiplexer for each outgoing bit line." Garnett et al. does not teach this limitation. Specifically, Garnett teaches a bridge (fig. 1, 12) that couples to multiple output bit lines (fig. 2, 22, 24, 26). However, the bridge (fig. 1, 12) only uses one multiplexer (fig. 9, 143).

The use of a mutliplexer for each outgoing bit line as required in claim 11 provides a configurable high-speed connection at each intersection of "a plurality of busses" and "at least one cross-bus." Applicants submit that using only one multiplexer in a bridge as taught in Garnett would substantially change performance and control of each bridge. For at least these reasons individually or in combination, applicants submit claim 11 is allowable over the cited art.

Claims 12-14 depend on independent claim 11. Applicants respectfully submit that claim 11 and its dependent claims 12-14 are allowable over the cited art for the reasons given above.

Added Claims

Claims 16-24 have been added. Independent claim 16 recites in part, "local intersect busses are coupled to each of the local memory busses by four multiplexers at each intersection." Applicant cannot find the above limitation in the cited art. Specifically, applicants' submit that Garnett et al. does not teach local memory busses coupled to local intersecting busses by four multiplexers at each intersection. For at least these reasons, applicants submit that independent claim 16 and its dependent claims 17-24 are allowable over the cited art.

Conclusion

In the course of the foregoing discussions, applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

Applicant submits that this response constitutes a complete response to all of the issues raised in the office action of January 8, 2003. Applicant has responded to the various rejections under 35 USC §102(b) and §103. In view of the foregoing amendments and remarks, applicant submits that all pending claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. The examiner is invited to contact the undersigned if a telephone interview might prove helpful in resolving this application.

If any fees are inadvertently omitted or if any additional fees are required or have been overpaid, please appropriately charge or credit those fees to Conley Rose, P.C. Deposit Account Number 03-2769/5201-20400/DJK.

Respectfully submitted,

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